# MPF4392, MPF4393

Preferred Devices

# **JFET Switching Transistors**

# **N-Channel – Depletion**

## Features

• Pb-Free Packages are Available\*

### **MAXIMUM RATINGS**

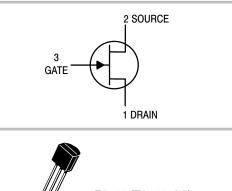
Rating	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DS</sub>	30	Vdc
Drain-Gate Voltag	V <sub>DG</sub>	30	Vdc
Gate-Source Voltage	V <sub>GS</sub>	30	Vdc
Forward Gate Current	I <sub>G(f)</sub>	50	mAdc
Total Device Dissipation @ T <sub>A</sub> = 25°C Derate above 25°C	P <sub>D</sub>	350 2.8	mW mW/°C
Operating and Storage Channel Temperature Range	T <sub>channel</sub> , T <sub>stg</sub>	-65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.



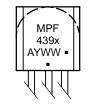
# **ON Semiconductor®**

### http://onsemi.com





### **MARKING DIAGRAM**



MPF439x = Device Code

	x = 2 or 3
А	<ul> <li>Assembly Location</li> </ul>
Y	= Year

= Work Week

WW

• = Pb-Free Package (Note: Microdot may be in either location)

### ORDERING INFORMATION

ORDERI	ORDERING INFORMATION				
Device	Package	Shipping <sup>†</sup>			
MPF4392	TO-92	1000 Units / Bulk			
MPF4392G	TO-92 (Pb-Free)	1000 Units / Bulk			
MPF4393	TO-92	1000 Units / Bulk			
MPF4393G	TO–92 (Pb–Free)	1000 Units / Bulk			
MPF4393RLRP	TO-92	1000 / Ammo Box			
MPF4393RLRPG	TO-92 (Pb-Free)	1000 / Ammo Box			

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Preferred devices are recommended choices for future use and best overall value.

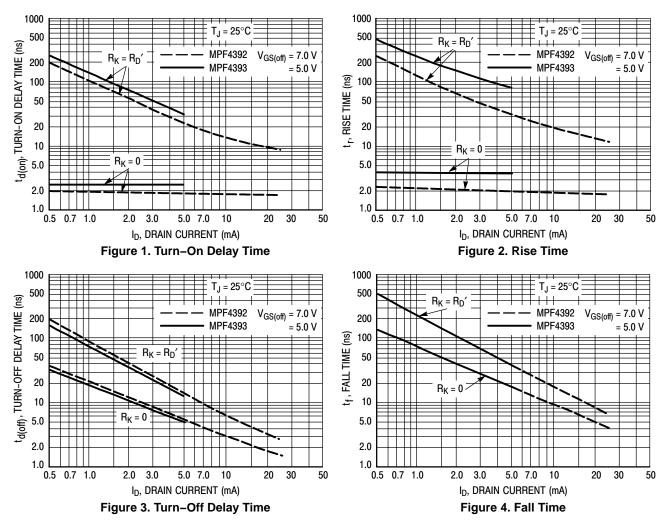
# MPF4392, MPF4393

# **ELECTRICAL CHARACTERISTICS** ( $T_A = 25^{\circ}C$ unless otherwise noted)

Characteristic		Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS					•	
Gate – Source Breakdown Voltage $(I_G = 1.0 \ \mu Adc, \ V_{DS} = 0)$		V <sub>(BR)GSS</sub>	30	-	-	Vdc
Gate Reverse Current ( $V_{GS}$ = 15 Vdc, $V_{DS}$ = 0) ( $V_{GS}$ = 15 Vdc, $V_{DS}$ = 0, $T_A$ = 100°C)		I <sub>GSS</sub>			1.0 0.2	nAdc μAdc
$ \begin{array}{l} \text{Drain-Cutoff Current} \\ (\text{V}_{\text{DS}} = 15 \ \text{Vdc}, \ \text{V}_{\text{GS}} = 12 \ \text{Vdc}) \\ (\text{V}_{\text{DS}} = 15 \ \text{Vdc}, \ \text{V}_{\text{GS}} = 12 \ \text{Vdc}, \ \text{T}_{\text{A}} = 100^{\circ}\text{C}) \end{array} $		I <sub>D(off)</sub>			1.0 0.1	nAdc µAdc
Gate Source Voltage (V <sub>DS</sub> = 15 Vdc, I <sub>D</sub> = 10 nAdc)	MPF4392 MPF4393	V <sub>GS</sub>	-2.0 -0.5		-5.0 -3.0	Vdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current (Note 1) $(V_{DS} = 15 \text{ Vdc}, V_{GS} = 0)$	MPF4392 MPF4393	I <sub>DSS</sub>	25 5.0		75 30	mAdc
Drain-Source On-Voltage $(I_D = 6.0 \text{ mAdc}, V_{GS} = 0)$ $(I_D = 3.0 \text{ mAdc}, V_{GS} = 0)$	MPF4392 MPF4393	V <sub>DS(on)</sub>			0.4 0.4	Vdc
Static Drain–Source On Resistance $(I_D = 1.0 \text{ mAdc}, V_{GS} = 0)$	MPF4392 MPF4393	r <sub>DS(on)</sub>			60 100	Ω
SMALL-SIGNAL CHARACTERISTICS			1	1		1
Forward Transfer Admittance $(V_{DS} = 15 \text{ Vdc}, I_D = 25 \text{ mAdc}, f = 1.0 \text{ kHz})$ $(V_{DS} = 15 \text{ Vdc}, I_D = 5.0 \text{ mAdc}, f = 1.0 \text{ kHz})$	MPF4392 MPF4393	y <sub>fs</sub>		17 12		mmhos
Drain–Source "ON" Resistance $(V_{GS} = 0, I_D = 0, f = 1.0 \text{ kHz})$	MPF4392 MPF4393	r <sub>ds(on)</sub>			60 100	Ω
Input Capacitance ( $V_{GS}$ = 15 Vdc, $V_{DS}$ = 0, f = 1.0 MHz)		C <sub>iss</sub>	_	6.0	10	pF
Reverse Transfer Capacitance $(V_{GS} = 12 \text{ Vdc}, V_{DS} = 0, f = 1.0 \text{ MHz})$ $(V_{DS} = 15 \text{ Vdc}, I_D = 10 \text{ mAdc}, f = 1.0 \text{ MHz})$		C <sub>rss</sub>		2.5 3.2	3.5 -	pF
SWITCHING CHARACTERISTICS						
Rise Time (See Figure 2) $(I_{D(on)} = 6.0 \text{ mAdc})$ $(I_{D(on)} = 3.0 \text{ mAdc})$	MPF4392 MPF4393	t <sub>r</sub>		2.0 2.5	5.0 5.0	ns
Fall Time (See Figure 4) $(V_{GS(off)} = 7.0 \text{ Vdc})$ $(V_{GS(off)} = 5.0 \text{ Vdc})$	MPF4392 MPF4393	t <sub>f</sub>		15 29	20 35	ns
Turn–On Time (See Figures 1 and 2) $(I_{D(on)} = 6.0 \text{ mAdc})$ $(I_{D(on)} = 3.0 \text{ mAdc})$	MPF4392 MPF4393	t <sub>on</sub>		4.0 6.5	15 15	ns
Turn–Off Time (See Figures 3 and 4) $(V_{GS(off)} = 7.0 \text{ Vdc})$ $(V_{GS(off)} = 5.0 \text{ Vdc})$	MPF4392 MPF4393	t <sub>off</sub>		20 37	35 55	ns

1. Pulse Test: Pulse Width  $\leq$  300 µs, Duty Cycle  $\leq$  3.0%.

# MPF4392, MPF4393



### **TYPICAL SWITCHING CHARACTERISTICS**

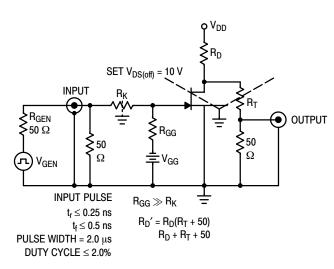


Figure 5. Switching Time Test Circuit

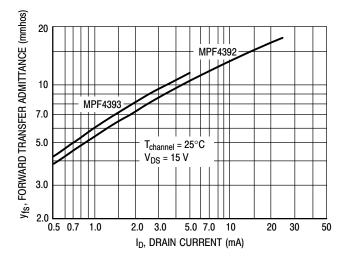


Figure 6. Typical Forward Transfer Admittance

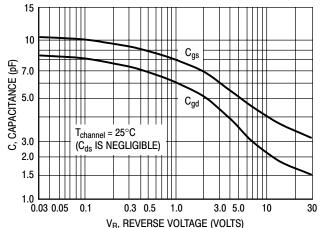
### NOTE 1

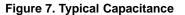
The switching characteristics shown above were measured using a test circuit similar to Figure 5. At the beginning of the switching interval, the gate voltage is at Gate Supply Voltage ( $-V_{GG}$ ). The Drain–Source Voltage ( $V_{DS}$ ) is slightly lower than Drain Supply Voltage ( $V_{DD}$ ) due to the voltage divider. Thus Reverse Transfer Capacitance ( $C_{rss}$ ) or Gate–Drain Capacitance ( $C_{gd}$ ) is charged to  $V_{GG} + V_{DS}$ .

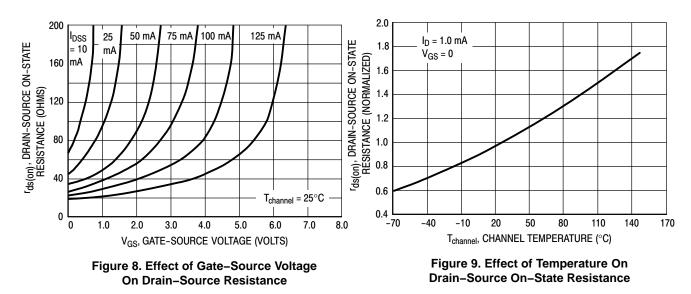
During the turn–on interval, Gate–Source Capacitance ( $C_{gs}$ ) discharges through the series combination of  $R_{Gen}$  and  $R_K$ .  $C_{gd}$  must discharge to  $V_{DS(on)}$  through  $R_G$  and  $R_K$  in series with the parallel combination of effective load impedance ( $R'_D$ ) and Drain–Source Resistance ( $r_{ds}$ ). During the turn–off, this charge flow is reversed.

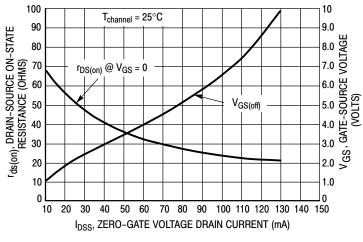
Predicting turn–on time is somewhat difficult as the channel resistance  $r_{ds}$  is a function of the gate–source voltage. While  $C_{gs}$  discharges,  $V_{GS}$  approaches zero and  $r_{ds}$  decreases. Since  $C_{gd}$  discharges through  $r_{ds}$ , turn–on time is non–linear. During turn–off, the situation is reversed with  $r_{ds}$  increasing as  $C_{gd}$  charges.

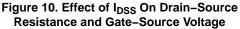
The above switching curves show two impedance conditions: 1)  $R_K$  is equal to  $R_D'$  which simulates the switching behavior of cascaded stages where the driving source impedance is normally the load impedance of the previous stage, and 2)  $R_K = 0$  (low impedance) the driving source impedance is that of the generator.











### NOTE 2

The Zero–Gate–Voltage Drain Current (I<sub>DSS</sub>), is the principle determinant of other J–FET characteristics. Figure 10 shows the relationship of Gate–Source Off Voltage (V<sub>GS(off)</sub>) and Drain–Source On Resistance ( $r_{ds(on)}$ ) to I<sub>DSS</sub>. Most of the devices will be within ±10% of the values shown in Figure 10. This data will be useful in predicting the characteristic variations for a given part number.

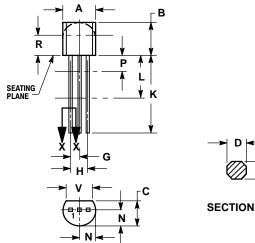
For example: Unknown

 $r_{ds(on)}$  and  $V_{GS}$  range for an MPF4392

The electrical characteristics table indicates that an MPF4392 has an  $I_{DSS}$  range of 25 to 75 mA. Figure 10 shows  $r_{ds(on)} = 52 \ \Omega$  for  $I_{DSS} = 25 \ mA$  and 30  $\Omega$  for  $I_{DSS}$  75 mA. The corresponding  $V_{GS}$  values are 2.2 V and 4.8 V.

### PACKAGE DIMENSIONS

TO-92 (TO-226) CASE 29-11 **ISSUE AL** 







NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI 1. Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH. CONTOUR OF PACKAGE BEYOND DIMENSION R 2
- 3. IS UNCONTROLLED. LEAD DIMENSION IS UNCONTROLLED IN P AND
- 4. BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.175	0.205	4.45	5.20
В	0.170	0.210	4.32	5.33
С	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
Н	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
Κ	0.500		12.70	
L	0.250		6.35	
Ν	0.080	0.105	2.04	2.66
Ρ		0.100		2.54
R	0.115		2.93	
×	0.135		3.43	

STYLE 5: PIN 1. DRAIN

2. SOURCE

3. GATE

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